Magnavox

GOVERNMENT & INDUSTRIAL ELECTRONICS COMPANY

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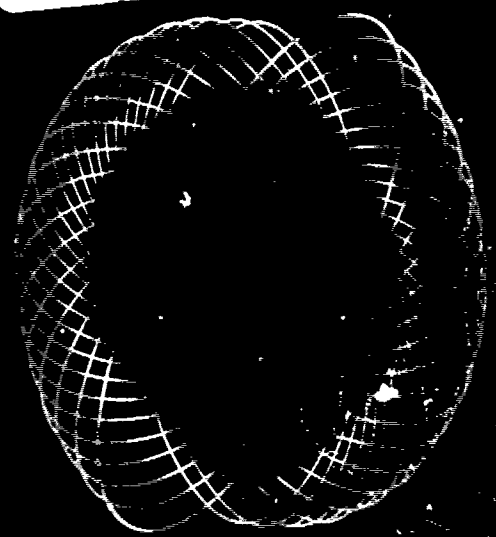

ELECTRO OPTICAL SYSTEMS

ADVANCED PRODUCTS DIVISION

FINAL REPORT

DETECTOR TEST BED,

Magnavox
GOVERNMENT & INDUSTRIAL ELECTRONICS COMPANY
ADVANCED PRODUCTS DIVISION / ELECTRO-OPTICAL SYSTEMS
46 INDUSTRIAL AVENUE MAHWAH, N.J. 07430

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SUMMARY

A detector test bed has been designed, fabricated and tested. Some portions of an early model of the HHTV (AN/PAS-7) were incorporated into the design. The goal of the design was to obtain a test bed for the evaluation of thermoelectrically cooled 3 to 5 μ PbSeTe photovoltaic detectors. Optics, scanner and some electronics were used from the GFE HHV. All other electrical and mechanical features were designed and developed on the program. In the absence of fully developed detectors, the preamplifiers were designed to interface with a PV detector whose parameters and characteristics were based upon theoretical values. The system is designed to furnish a non-interlaced parallel scan for detector arrays up to 48 elements and element sizes representative of the state of the art. Space was kept available in the opto-mechanical design to allow incorporation of a 2:1 interlace capability at a later date. A forced air cooling concept was furnished to handle the expected cooler power input to the detector (typically 25 watts). A water cooled detector mount was also designed but not fabricated. Test points for individual channels and other special system features will be discussed in the body of this report. Preamplifiers could be supplied to furnish a broader test bed potential, namely, to allow testing of 3 to 5 micron TE cooled HgCdTe P.C. detectors. Some interface work and system integration would be required before full compatibility of the HgCdTe detectors is obtainable.

Since a 48 element PbSeTe detector having reasonably representative parameters and characteristics was not available, detailed test data on that detector are not available. Tests did show that the available detector array had apparently degraded by about a factor of 10, even though

cooling and vacuum appeared satisfactory. However, the detector was mounted, wired and integrated into the system. Preamplifier compatibility was demonstrated and overall system debugging performed. Imaging was accomplished at poor sensitivity but extensive quantitative tests and data are not available.

CONCLUSION AND RECOMMENDATIONS

The basic program goals of the test bed design and development effort have been obtained. The test bed is compatible with PbSeTe PV 3-5μdetector arrays. It has the versatility and potential of testing other 3-5μdetector arrays with the incorporation of appropriate preamplifiers for electronic interface.

It is recommended that the test bed be used to complete the evaluation of PbSeTe type detectors and necessary modifications be made to allow testing of other types (eg. HgCdTe). It is also recommended that the water cooled detector mount be fabricated. This could furnish a capability which would allow greater versatility in testing since the base temperature becomes controllable as a function of the coolant temperature and thus variable cold face temperatures are available. This feature could also make it possible to test an otherwise unusable array where the TE cooler is not furnishing proper cooling levels. Incorporation of an interlace capability would also increase the utility of the test bed.

SECTION I

3-5 MICRON DETECTOR TEST BED

1.1 GENERAL

The 3-5 micron test bed is a real time thermal imaging system designed for the evaluation of PbSeTe detectors. It consists of an infrared lens, a parallel beam scan mirror and signal processing to either an X-Y CRT display or a 1 inch CRT. The objective lens is a Si-Ge-Si triplet of a quality to allow test of detector elements of sizes down to a few thousanths of an inch.

1.2 SYSTEM DESCRIPTION

The scanner uses a front surfaced aluminum mirror driven by a brushless torque motor to yield either 15 or 30 frames, 2:1 format scan. Signals from the 48 detector elements under test are processed through 48 signal processing channels consisting of low noise preamplifiers and postamplifiers. These amplifiers are arranged with four channels per plug-incard. Each card has 8 trim potentiometers for adjustment of preamp AC gain and bandwidth.

The postamplifier output from each card is monitored at the video connector on the front panel. Selection of the desired channel output is achieved by manipulation of the two rotary switches on the panel. With both switches in the "logic on" position, the multiplexers and multiplexer logic are active and the system is in the imaging mode. After rotating the amplifier card switch one position clockwise (from the Logic on position) the outputs of the first two cards (channels 1-8) are accessible by rotating the amplifier switch through positions 1-8.

The remaining channels are addressed in a similar fashion by advancing the amplifier card switch to select the desired group of 8 channels and the amplifier switch to select the desired channel within the group. When the system is used in this fashion, the viewer portion is disabled and the scan mirror switched off so the system is in a stare mode.

Provisions are provided on the front panel for Remote Video gain, remote horizontal, vertical and video. Brightness, contrast, focus and ON/OFF are on

the viewer portion of the front panel.

a. The viewer is the handheld portion of the Viewer, Infrared AN/PAS-7 and is the primary unit of the system. The viewer support structure consists of a magnesium housing frame braised to the front panel to form a one piece baseplate providing the main structure and mounting surfaces for all internal subassemblies. The cover contains the silicon IR window for entrance of the IR energy to the scan mirror and objective lens. The IR window is tilted downward to minimize reflections.

b. Immediately behind the IR window (mounted on the viewer cover), a parallel beam scan mirror assembly is mounted. This consists of a scan mirror driven or oscillated by a torque motor with a five to one gear reduction and a flat spring "bounce" mechanism which provides a high duty cycle, linear scan with minimum power drain and an adjustable frame rate from 15 to 30 frames per second. The scan mirror assembly also contains the reference signal generator (1A5) and the scan motor drive (1A6) printed circuit boards. The scan mirror assembly is mounted and doweled to the viewer housing frame.

c. The three optical element objective lens assembly is axially located by temperature compensating spacers and mounted on silicon rubber rings in an aluminum housing. The objective lens assembly is mounted in a bored frame, integral with the viewer housing frame and adjusted through a radially positioned eccentric pin attached to the focus control lever on the front panel.

d. The video board (1A4), and the CRT (1V1) are above the scan mirror, objective lens and detector network assembly.

SECTION II

TECHNICAL DISCUSSION

2.1 PURPOSE

The optic systems of the AN/PAS-7 (See Figure 1) are designed to provide an overall system magnification of 2.3. The purpose of the parallel beam scan mirror and objective lens optic system is to scan and focus the IR energy viewed through the IR window onto the 48-element detector array. The eyepiece optics in turn magnifies and focuses the image on the CRT display to accommodate the individual operator's eye.

2.2 SCANNING OPTICS

The scanning optics of the HTV consists of an IR window, a parallel beam scan mirror and an objective lens. The window is coated for maximum transmission in the 3 to 5 micron region and is protectively hard coated with silicon monoxide.

Immediately behind the IR window is the parallel beam scan mirror which bends the IR energy bundle 90° (degrees) through the objective lens to the detectors. The mirror is oscillated through plus and minus 3° to provide the plus and minus 6° of spacial scan for the 12° horizontal field of view. The mirror also provides a 6° vertical field of view.

The objective lens is a three-element 2.5 inch diameter lens system. The objective lens has a 2.5 inch focal length with a clear aperture of 2.5 inches and is a F/1 system. The focus of the objective lens is controlled by the FOCUS control lever which is connected to the lens system by eccentric pins and moves the lens system back and forth. This allows the operator to focus the objective lens system for maximum IR energy impinging upon the detector elements. The lens system is focusable from 8 meters to infinity (∞). The detector is mounted on an X-Y transfer table which provides a finer focus adjustment.

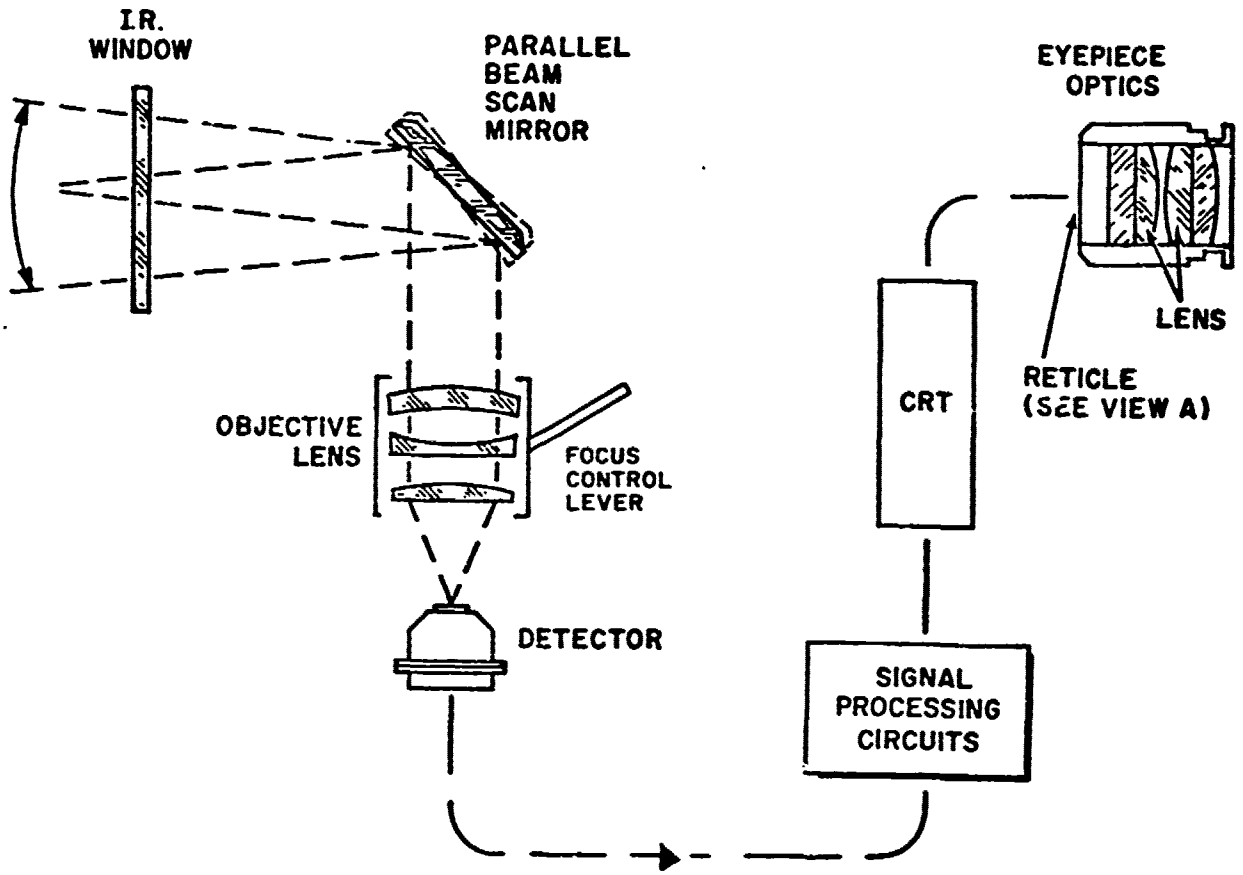

Figure 1. OPTICS SYSTEM

2.3 EYEPIECE OPTICS

The eyepiece optics is a 2-element system with a 1-1/8 inch focal length. The eyepiece lens focus is adjustable plus or minus 4 diopters to allow focus of the individual operator's eye to the CRT image display.

2.4 BLOCK DIAGRAM FUNCTIONING

The scene or target being viewed through the IR window is scanned by an oscillating parallel beam scan mirror. The infrared energy hitting the mirror is scanned through the objective lens assembly and focused onto a 48 element Pb SeTe detector array. The detectors are vertically mounted on the cold spot of the thermoelectric cooler so they will operate in their most sensitive region. The pre-amplifiers are designed to interface with the photovoltaic detectors and keep them at or near a zero bias condition. The voltage signals which result are amplified by the individual preamplifier associated with each detector of the array.

The 48 preamplifier output signals are further postamplified and applied to the inputs of six 8-channel multiplex switch integrated circuits (MX1 through MX6) driven in parallel. The six multiplex switches act like electronic stepping switches with each sampling 8 preamplifier outputs and converting them into a series string at the multiplex switches output (video output). The logic circuit generates output enable signals (OE1 through OE6) and binary count (8 count) each timed by the clock signal from the clock pulse generator. When the first multiplex switch (MX1) is enabled by the output enable signal (OE1), the binary counter provides 8 counts to activate each of the 8 switches in MX1 in sequence and the first 8 channels of video are added to the video output in series. Then MX1 is disabled and MX2 is enabled by OE2 and the next 8 channels of video (CH9 - CH16) are added to the video output of the next 8 counts of the binary counter. This sequence is continued until the 48 parallel signals are thus converted into a single series string video output. After the 48 channels have passed through the multiplex switches, the logic circuit enables the blanking

pulse generator to provide blanking during retrace. Then the sequence is repeated.

The video output of the multiplex switches is applied to the video amplifier through the contrast potentiometer. The blanking amplifier acts as the dc restorer while applying the video to the signal grid of the miniature CRT and provides blanking during retrace.

The vertical sweep for the CRT is derived from the logic circuit and applied to the vertical deflection plates of the CRT after shaping and amplification by the vertical sweep generator and amplifier. The horizontal sweep is initiated in the mirror position pickoff circuit and applied to the horizontal deflection plates of the CRT after shaping and amplification by the horizontal sweep generator and amplifier. The 1MHz oscillator signal is fed to the clock pulse generator which supplies timing (clock) signals for the logic and blanking circuits.

Primary power for the low voltage power supplies is provided by a 0 to 32 volt 2 ampere supply. The low voltage power supplies provide all the dc voltages required for the viewer electronic circuits and an ac primary voltage for the high voltage power supply. Switching in the dc to dc converter type low voltage power supply is controlled by a sync signal from the PS sync circuit and timed by the logic circuit to occur only during vertical retrace when the CRT display is blanked. The high voltage supply provides the anode, cathode, filament, and bias voltages required for the CRT.

2.5 DETECTOR-COOLER ASSEMBLY

The detector-cooler assembly contains a linear vertically oriented 48-element PbSeTe detector array mounted behind a sapphire window on the cold spot of the thermoelectric cooler. The thermoelectric cooler cools the detector array to approximately 170°K which is the area of high sensitivity for the

detector array elements. The thermoelectric cooler requires an input power of 30 watts (6 volts dc at 5 ampere). The detector is mounted on a block which acts as a heat sink for the TE cooler and which is in turn cooled by a fan assembly.

2.6 Detector Preamplifier

The detector preamplifier is shown schematically in Figure 2. It is comprised of three operational amplifier stages, with the first stage (A1) acting as a low noise moderate gain amplifier with a high input impedance. The RC coupling network between the first and second (A2) stage yields a high pass characteristic with a break frequency at 50 Hz. The second (A2) and third (A3) stages are of the low cost general purpose 741 type. The second stage provides a fixed gain of 31. By adjusting R8 of the variable RC coupling network between the second and third stages, the low pass filter characteristic can be adjusted from 4 KHz to 8.8 KHz for best signal to noise setting. The third stage has provision for variable gain. By adjusting R9 one can vary the stage gain from 1 to 10. The output is capacitively coupled.

The requirement for the preamplifier is that the noise be sufficiently low so that the system is basically detector noise limited and that the gain be sufficiently high so that the multiplexer noise not degrade signal fidelity. The PbSeTe detector noise, which is predominantly Johnson noise is approximately $25nv/\sqrt{Hz}$ at $170^{\circ}K$ with detector impedances averaging about 100K ohms.

The first stage gain is about 10 which will give a noise output of about $250nv/\sqrt{Hz}$. The feedback resistor ($1M\Omega$) contributes an

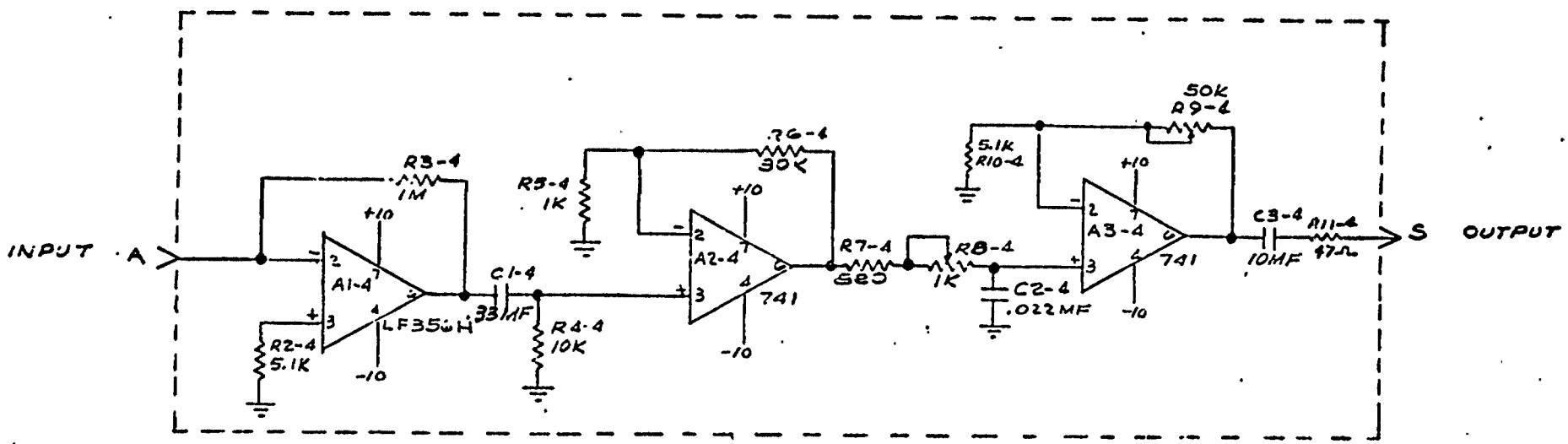

Figure 2. DETECTOR PREAMPLIFIER SCHEMATIC

additional 127nv/$\sqrt{HZ}$ for a total of 280nv/$\sqrt{HZ}$. Measured in a bandwidth that can vary from 4 to 8.8 KHz we have a total noise of about 17 to 26nv after the first stage, or a maximum noise level of 5.2 to 8 mv at the output of the last stage with maximum gain. These are acceptable noise levels to be presented to the multiplexers. Assuming an input capacity of 20pf the noise rise due to this capacity will occur at about 8KHz, but since the useable bandwidths are from 4 to 8.8KHz this source of additional noise will be largely filtered out.

The first stage uses an LF 356H Fet input, low noise operational amplifier, with an input impedance of 10^{12}ohms. It has an equivalent input noise voltage of typically 12nv/$\sqrt{HZ}$ at 1KHz. This adds less than 10% noise to the total.